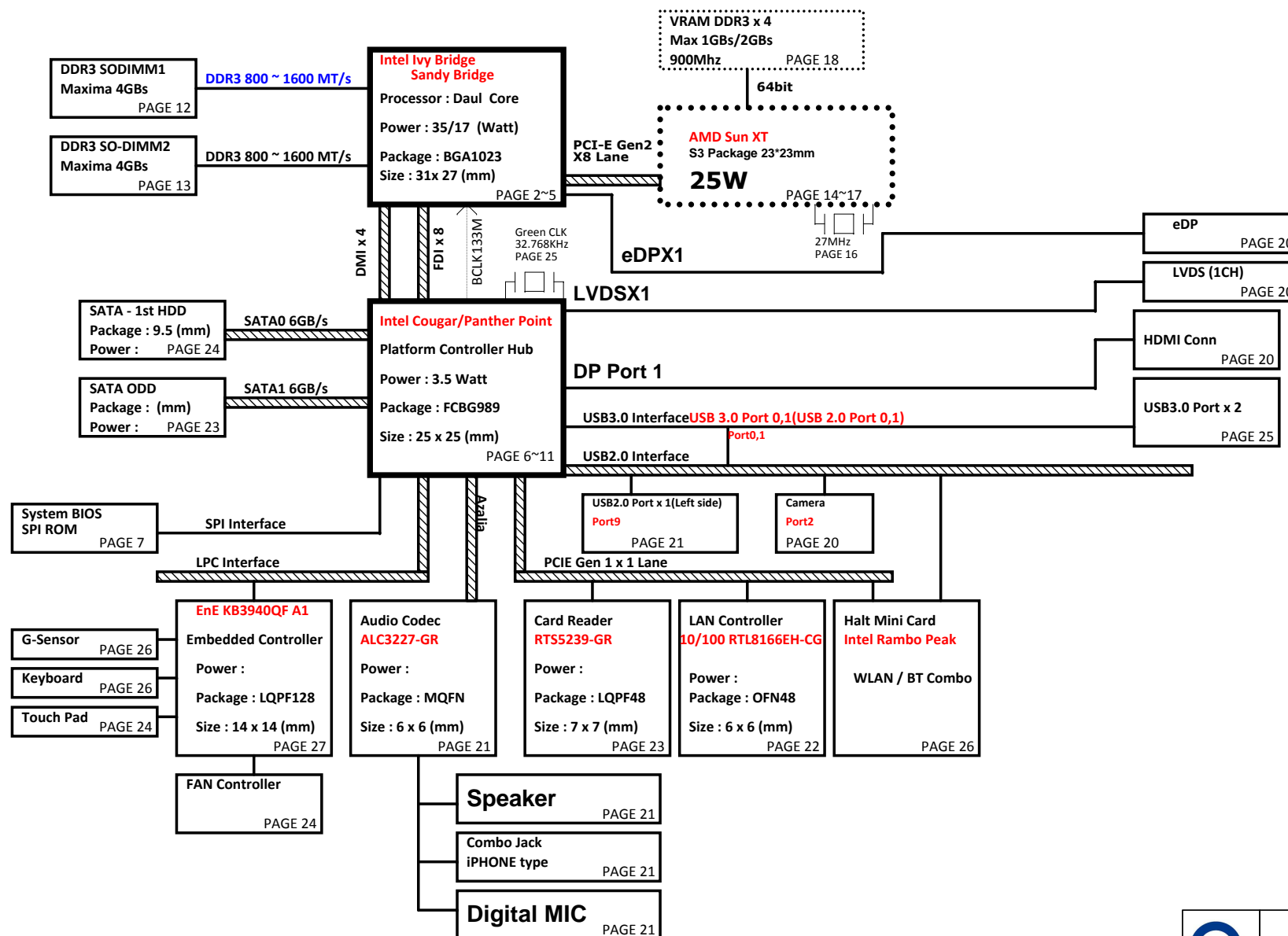


LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



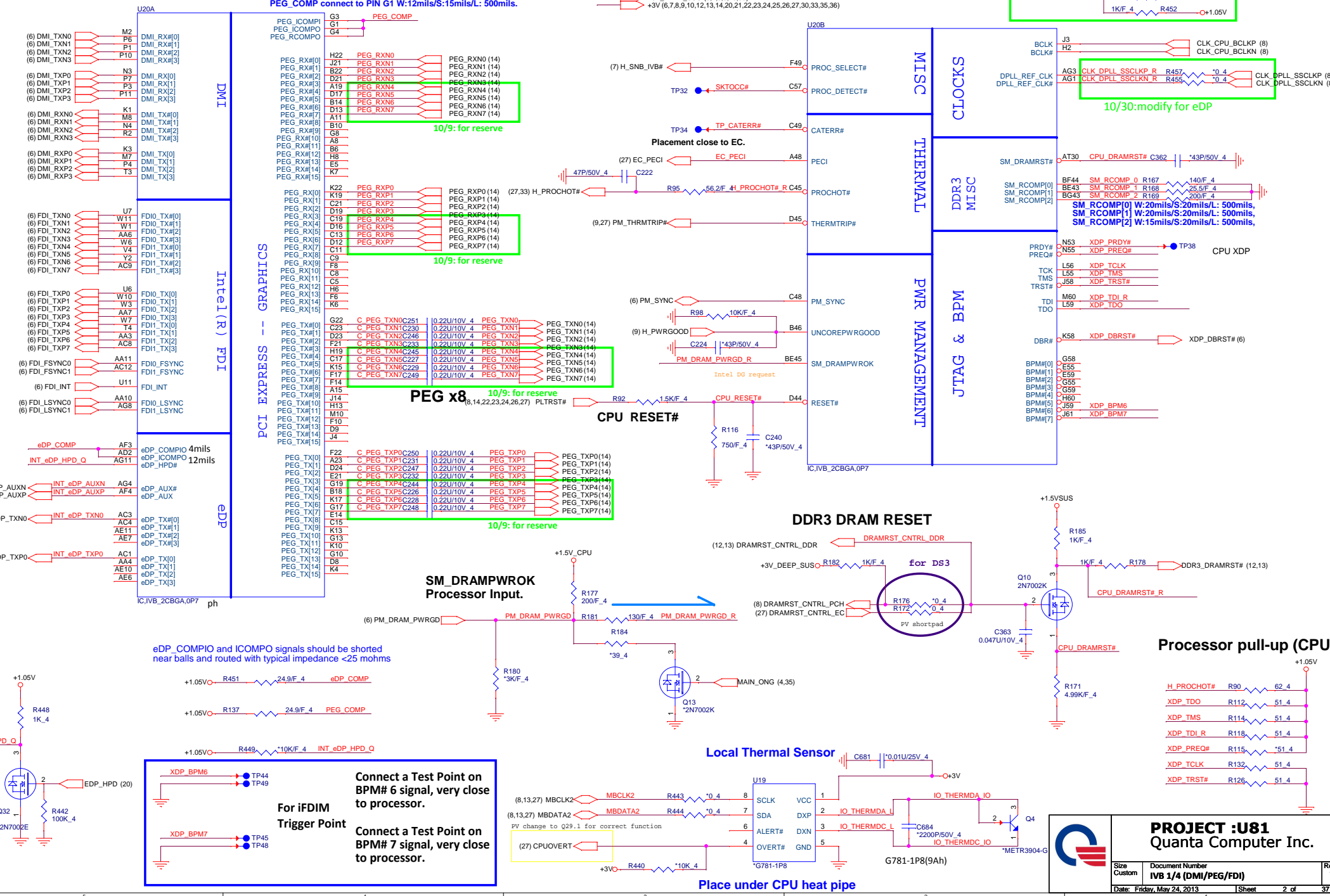
Ivy Bridge Processor (DMI,PEG,FDI)

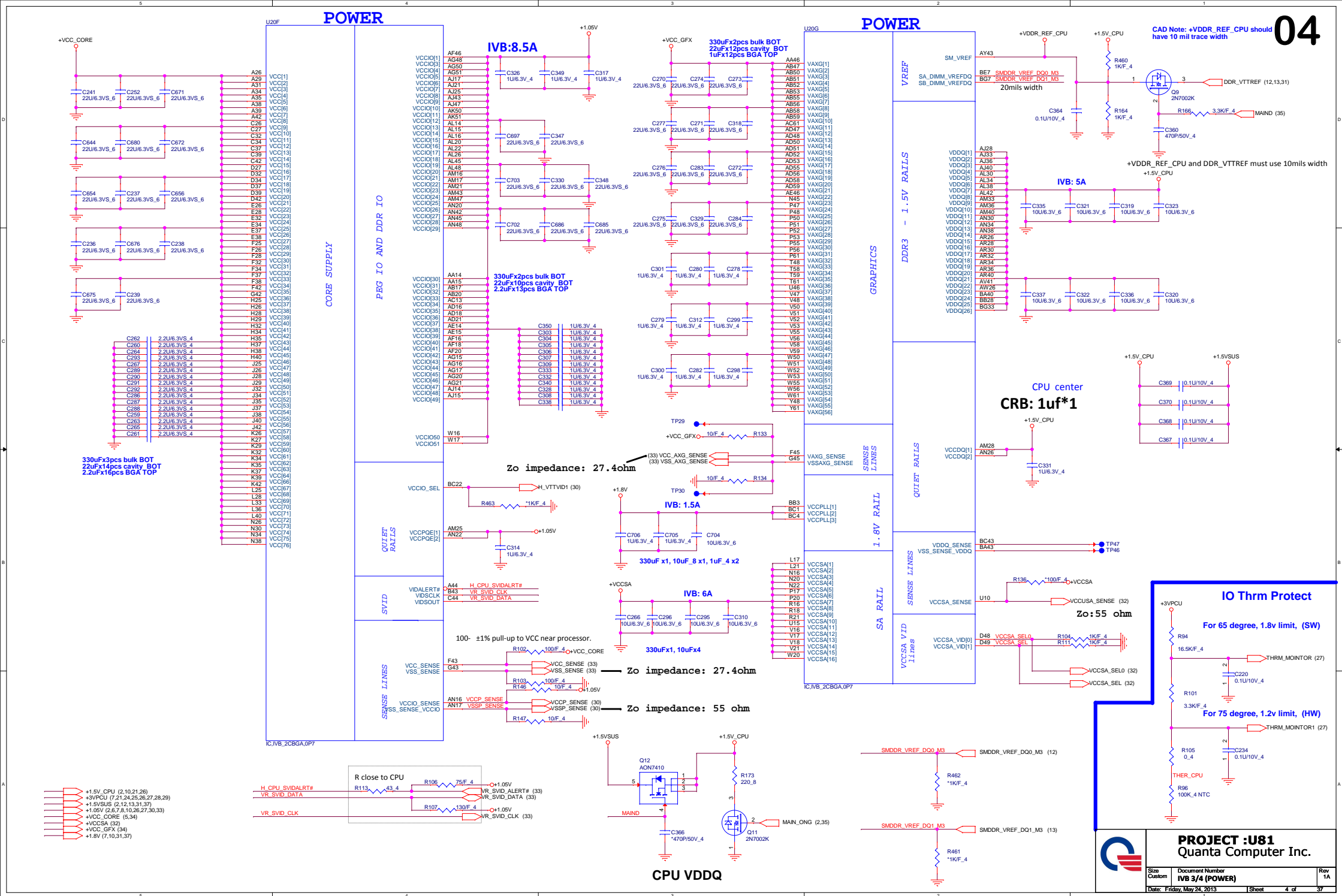
PEG_COMP connect to PIN G3/G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

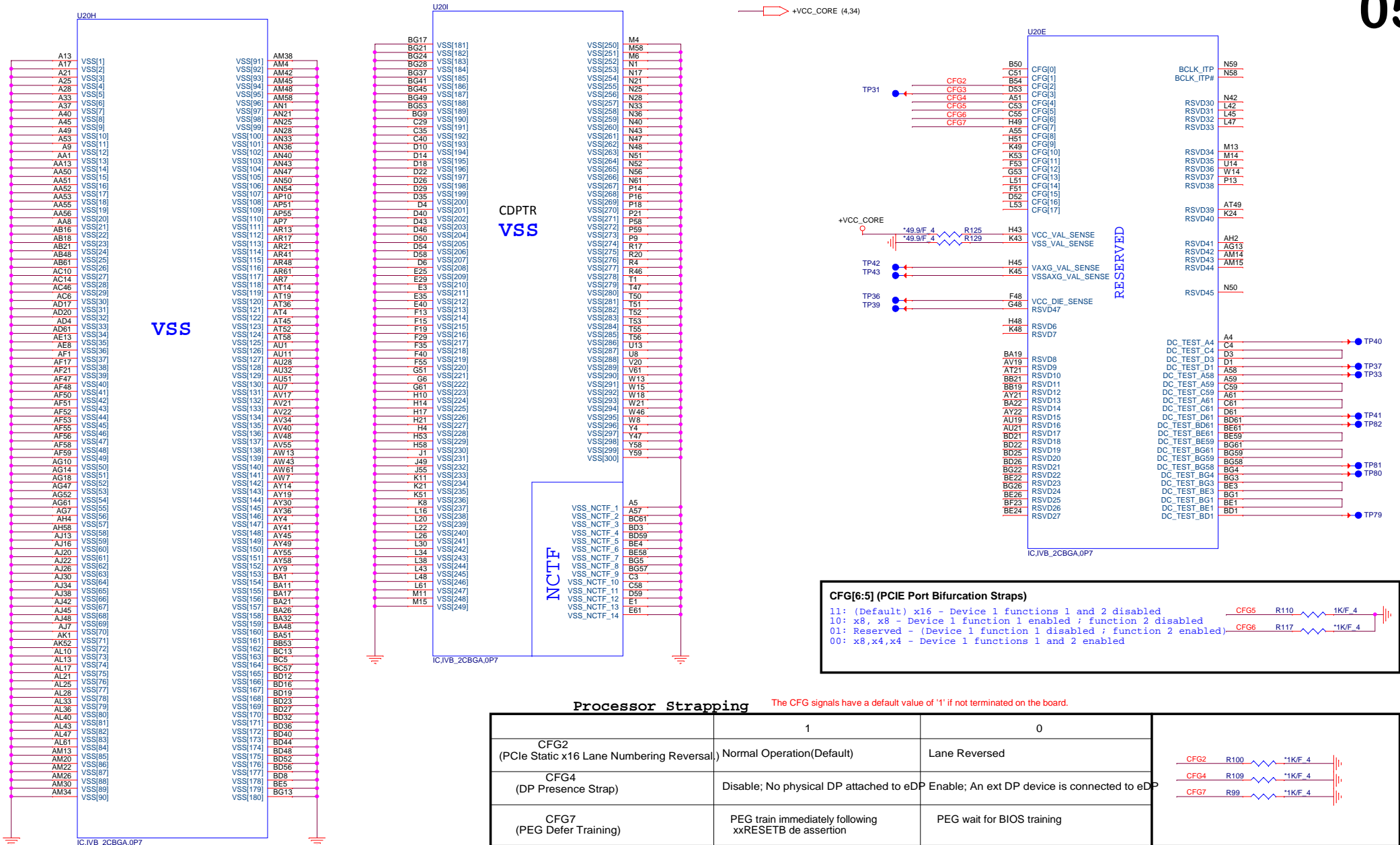
+1.5V_CPU (4,10,21,26)
+1.5VSUS (4,12,13,31,37)
+1.05V (4,6,7,8,10,26,27,30,33)
+3V_DEEP_SUS (6,7,8,9,10,35)
+3V (6,7,8,9,10,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36)

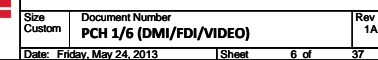
10/30:reserved for eDP

02

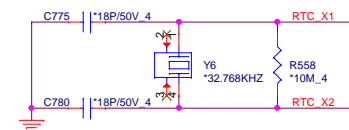






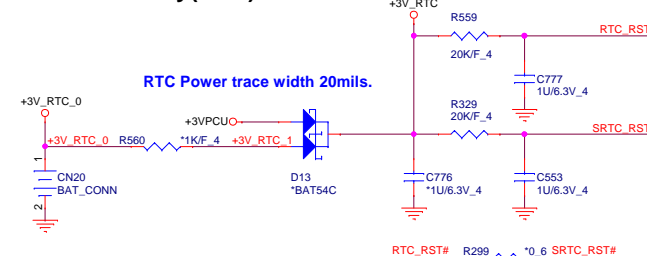


07

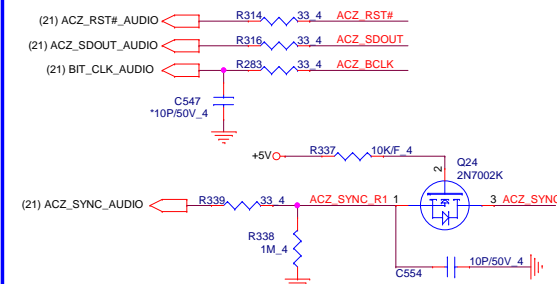


no stuff If use green Clock

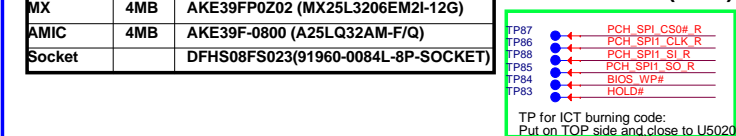
30mils



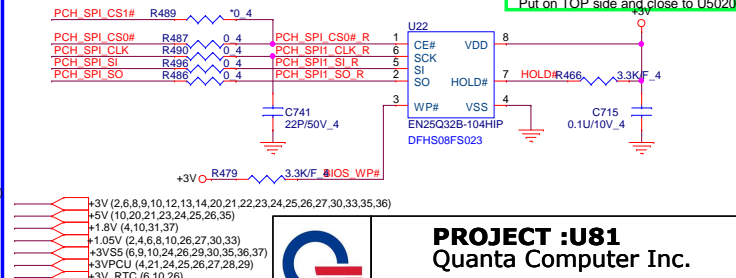
G)



PCH SPI ROM(CLG)



TP for ICT burning code:
Put on TOP side and close to U5020

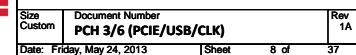


PROJECT :U81
Quanta Computer Inc.

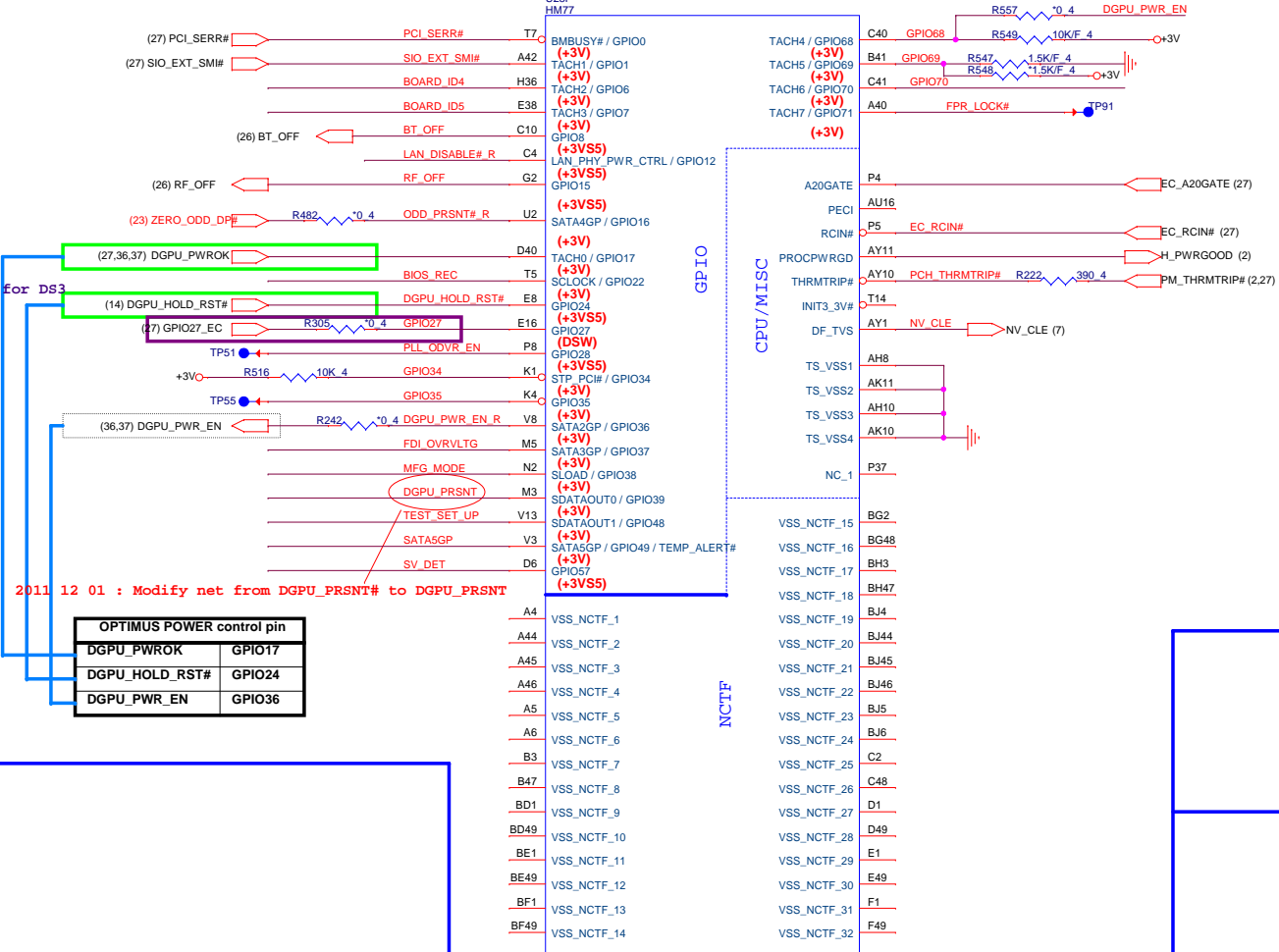
Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1A
Date: Friday, May 24, 2013	Sheet	7 of 37

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>1</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	1	LPC											
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ES1 strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										



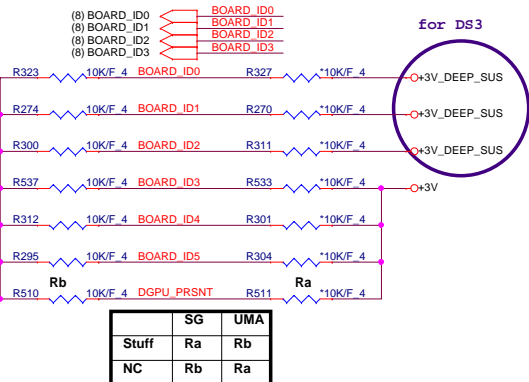
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

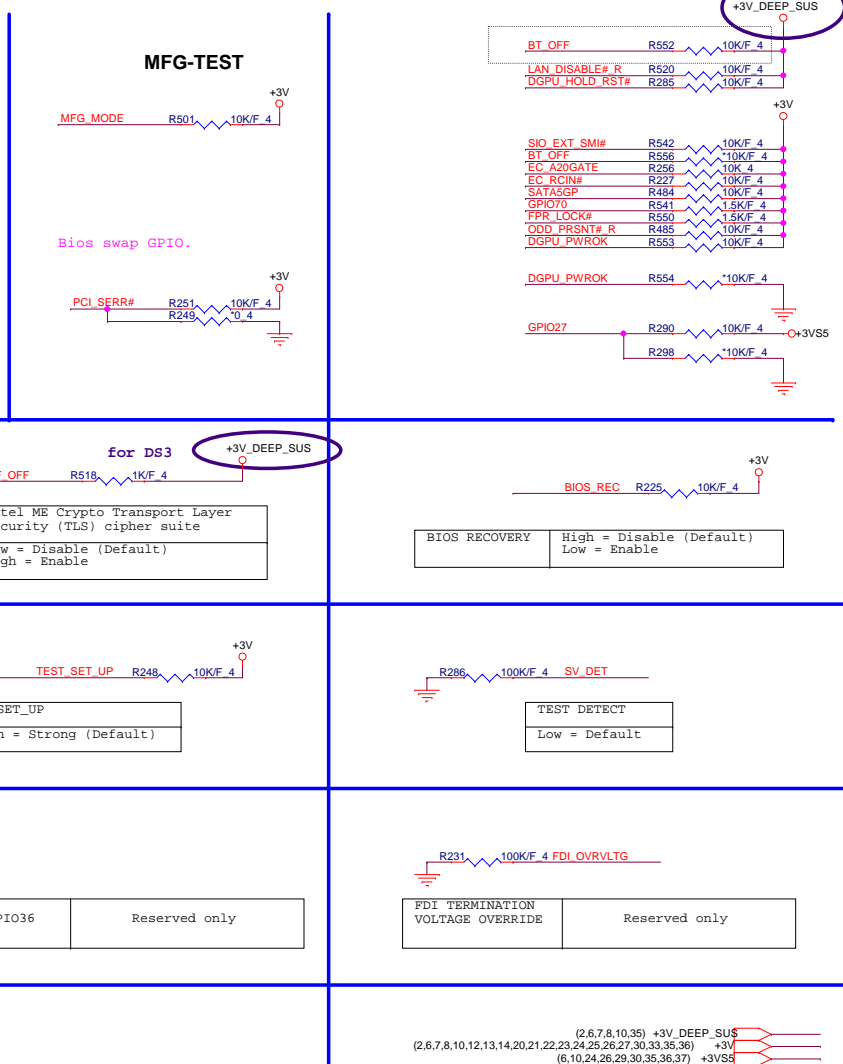
Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4 14": 0 15": 1	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0 UMA: 0 DIS: 1
U81 UMA	0	0	0	0	0	0
U81 SWG	0	0	0	0	0	1
14"	0	0	0	0	0	0
15.6"	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

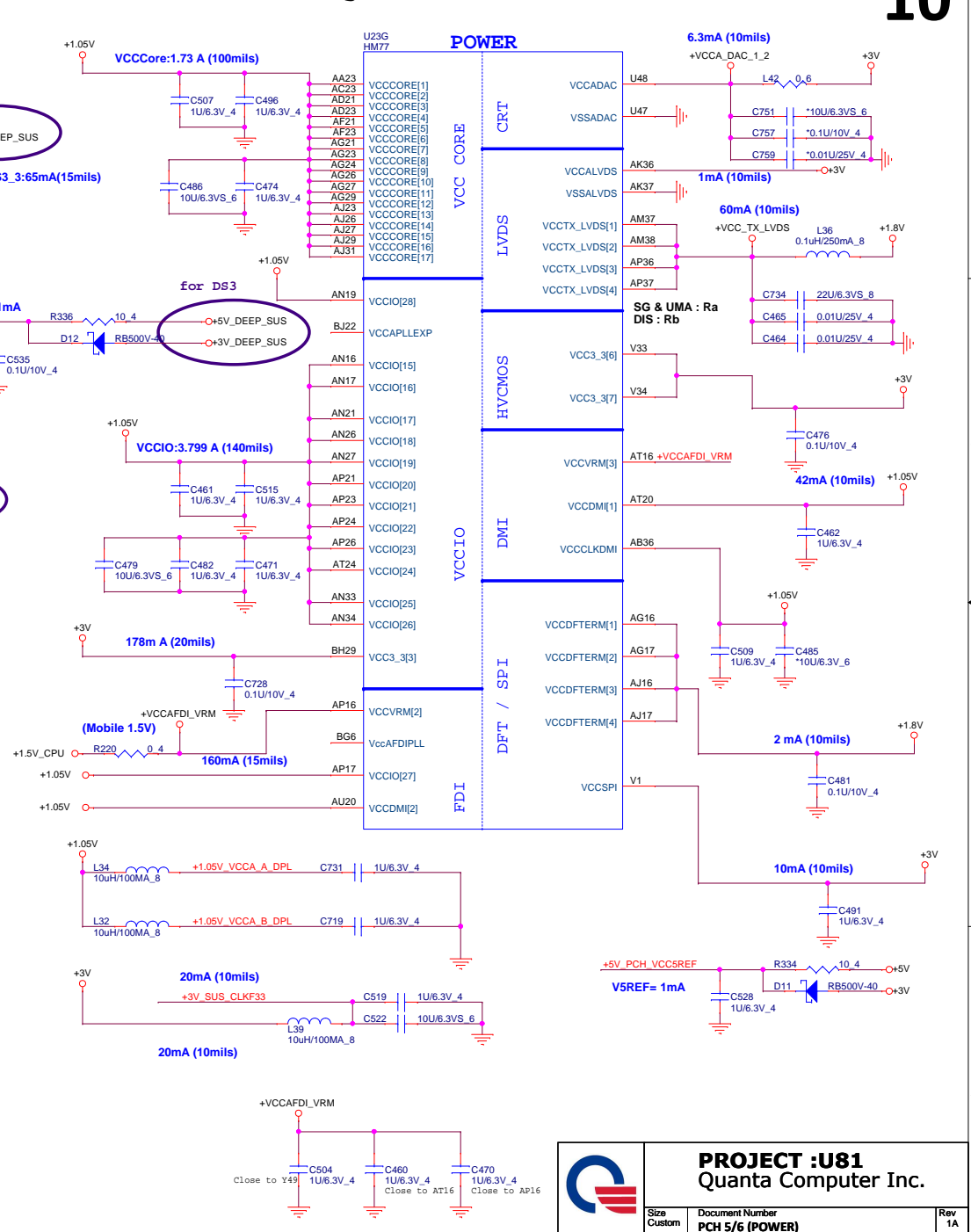
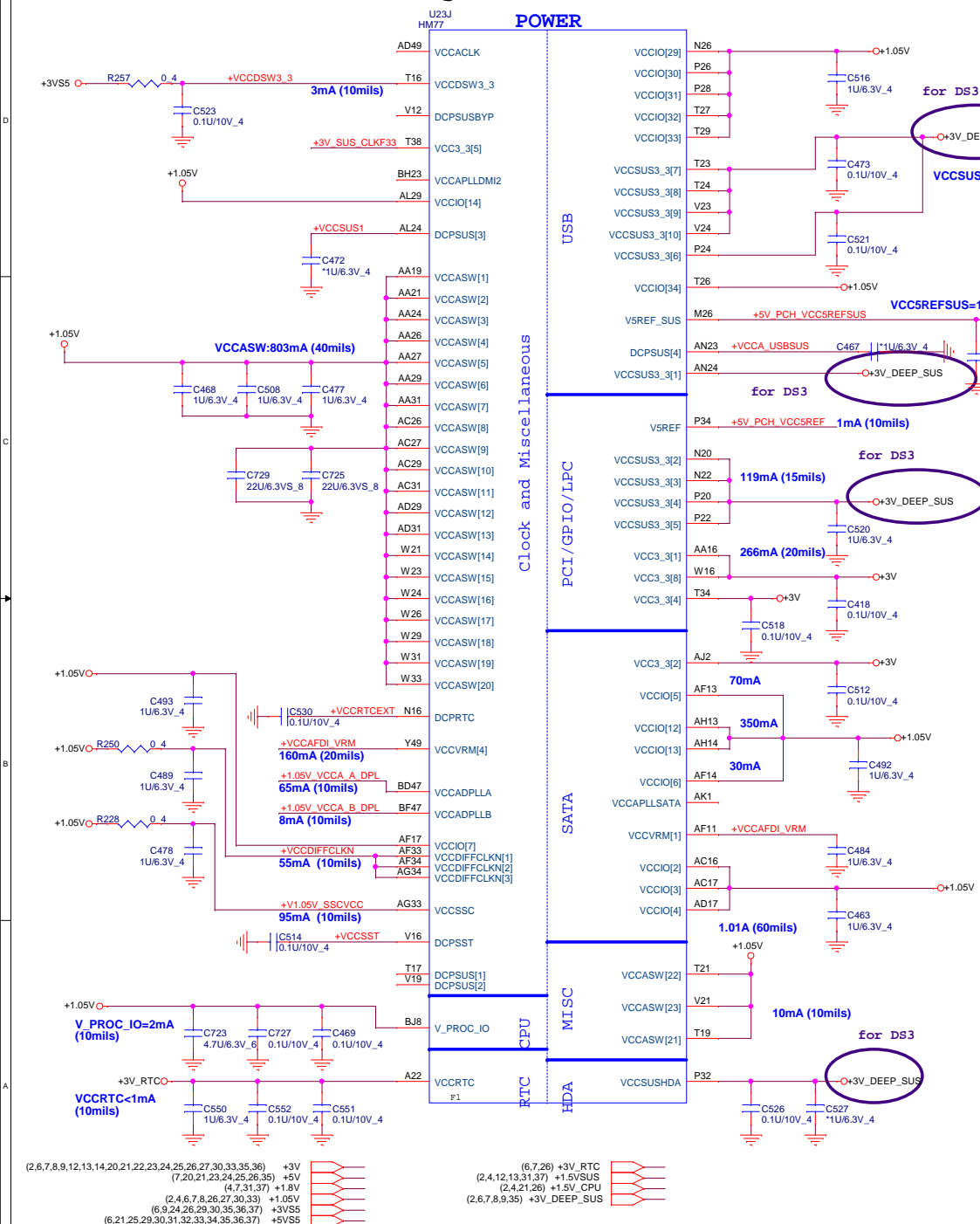
GPIO Pull-up/Pull-down(CLG)



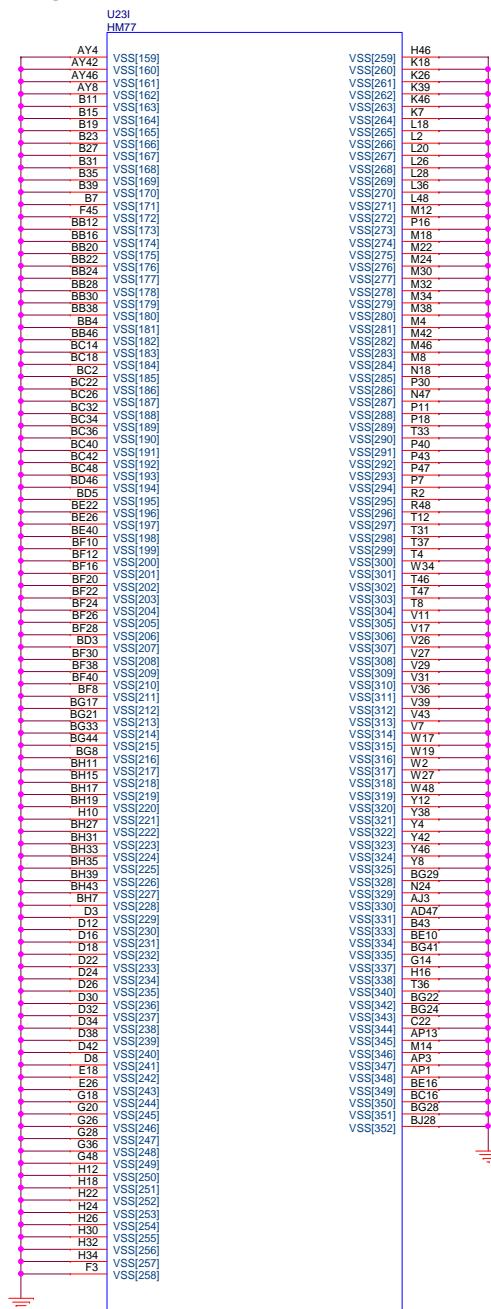
PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
Date: Friday, May 24, 2013	Sheet 9 of	37

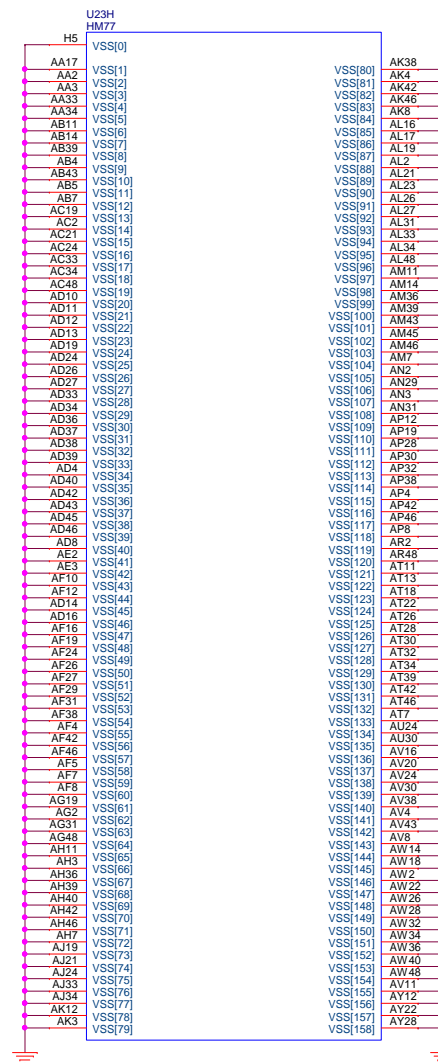
Cougar Point/Panther Point (POWER)

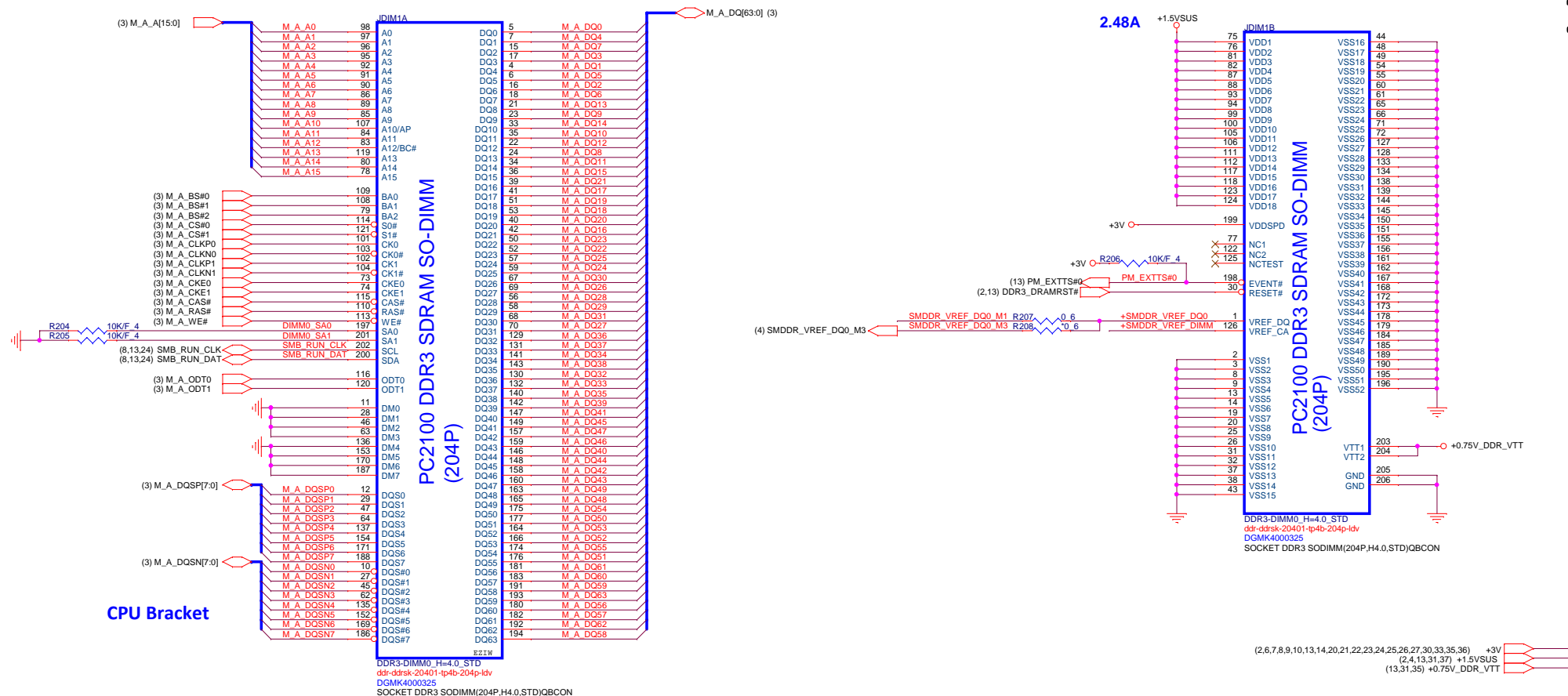


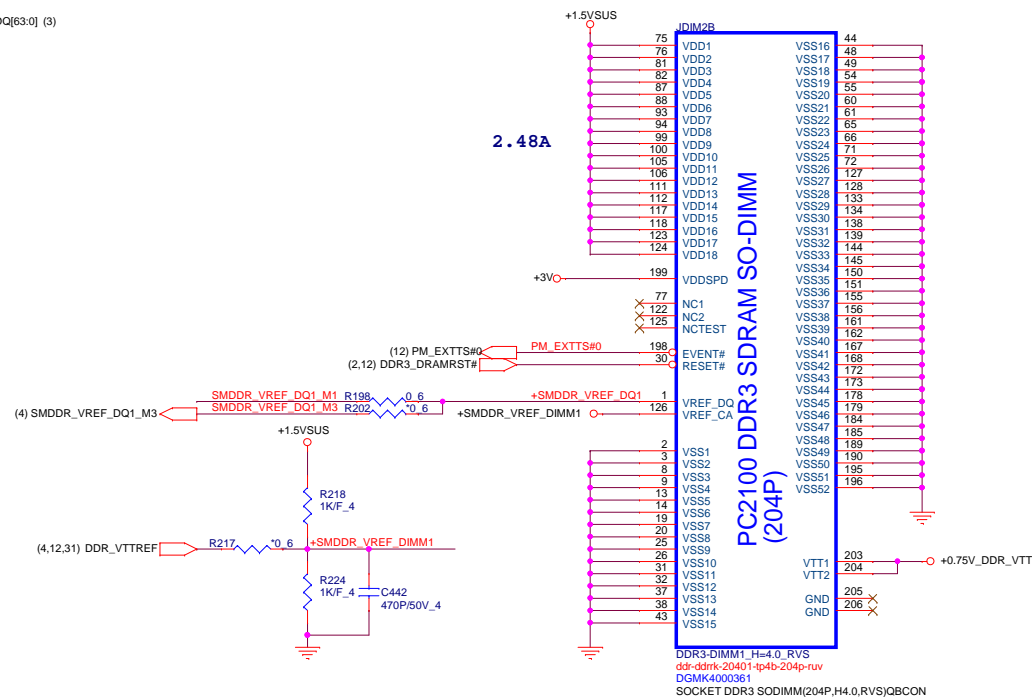
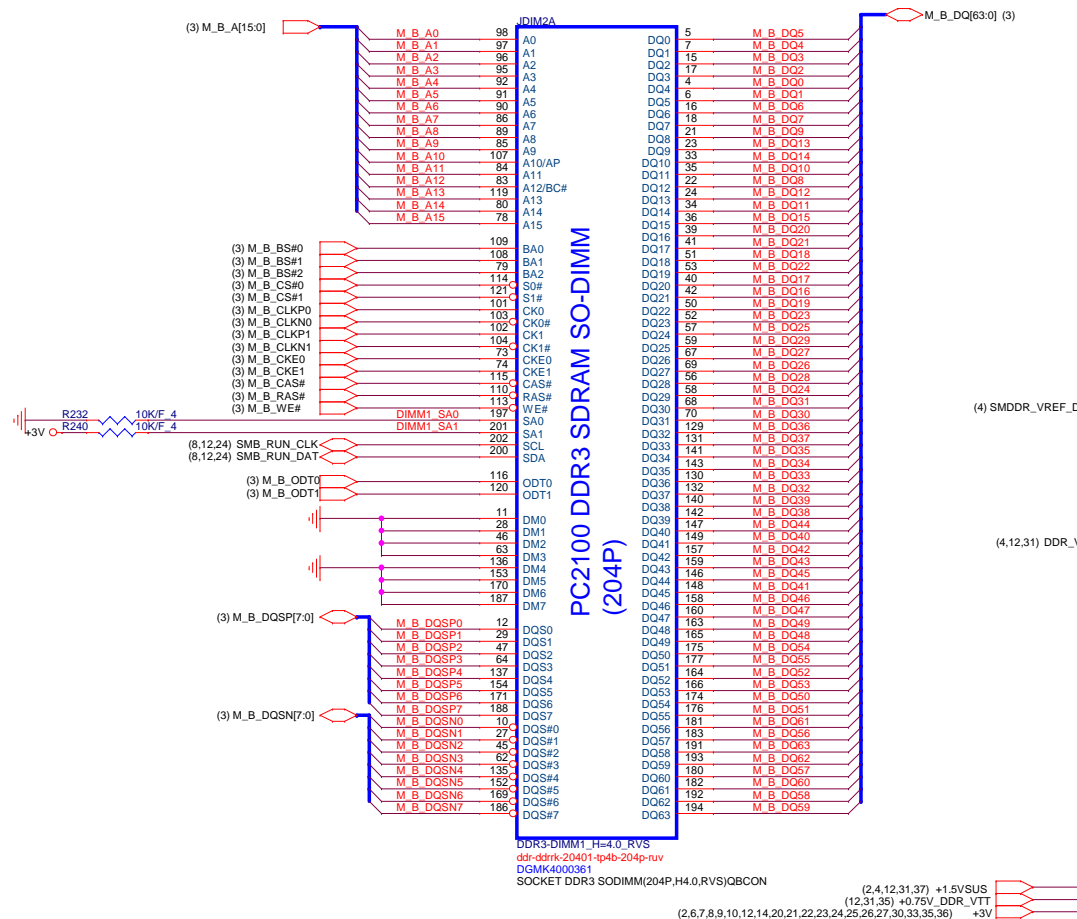
Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)

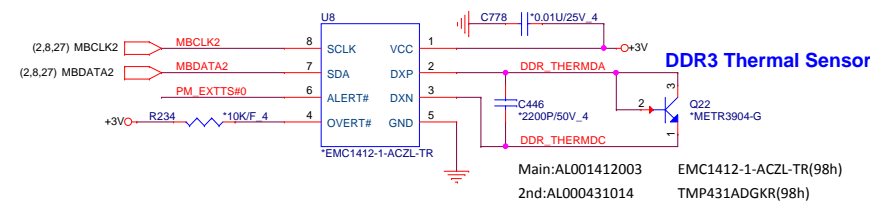




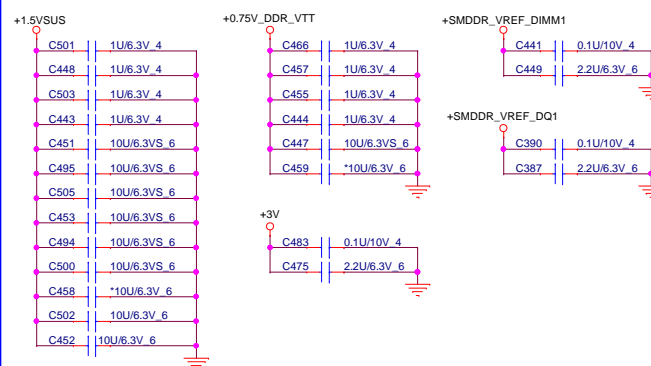


10/23:add for DDR Thermal Sensor

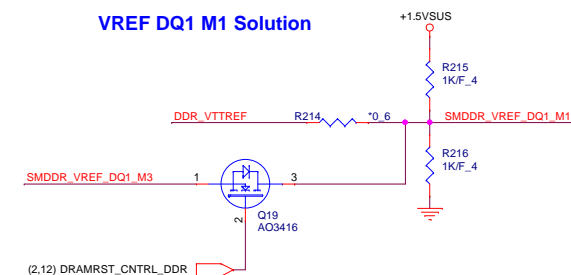
Local Thermal Sensor



Place these Caps near So-Dimm1.

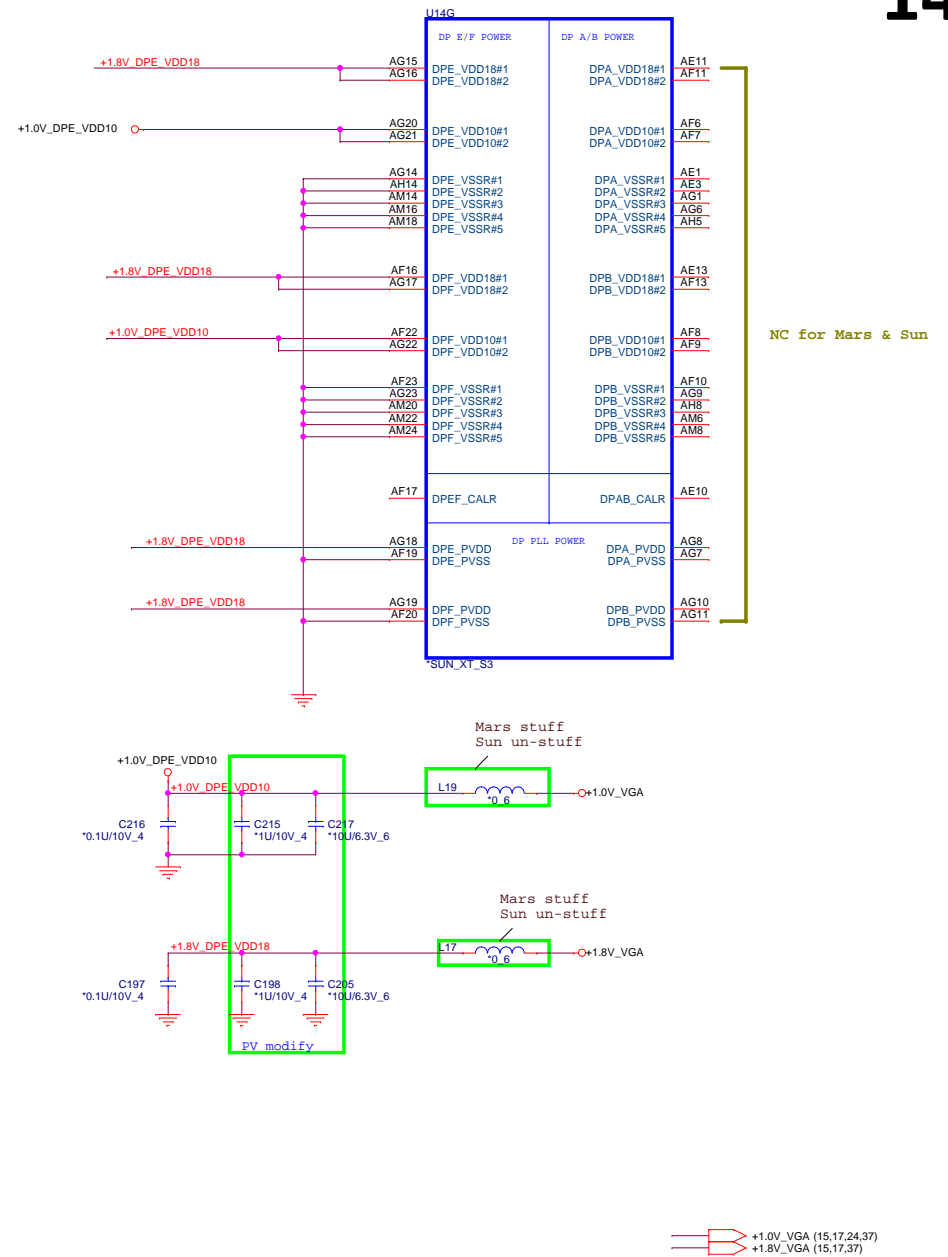
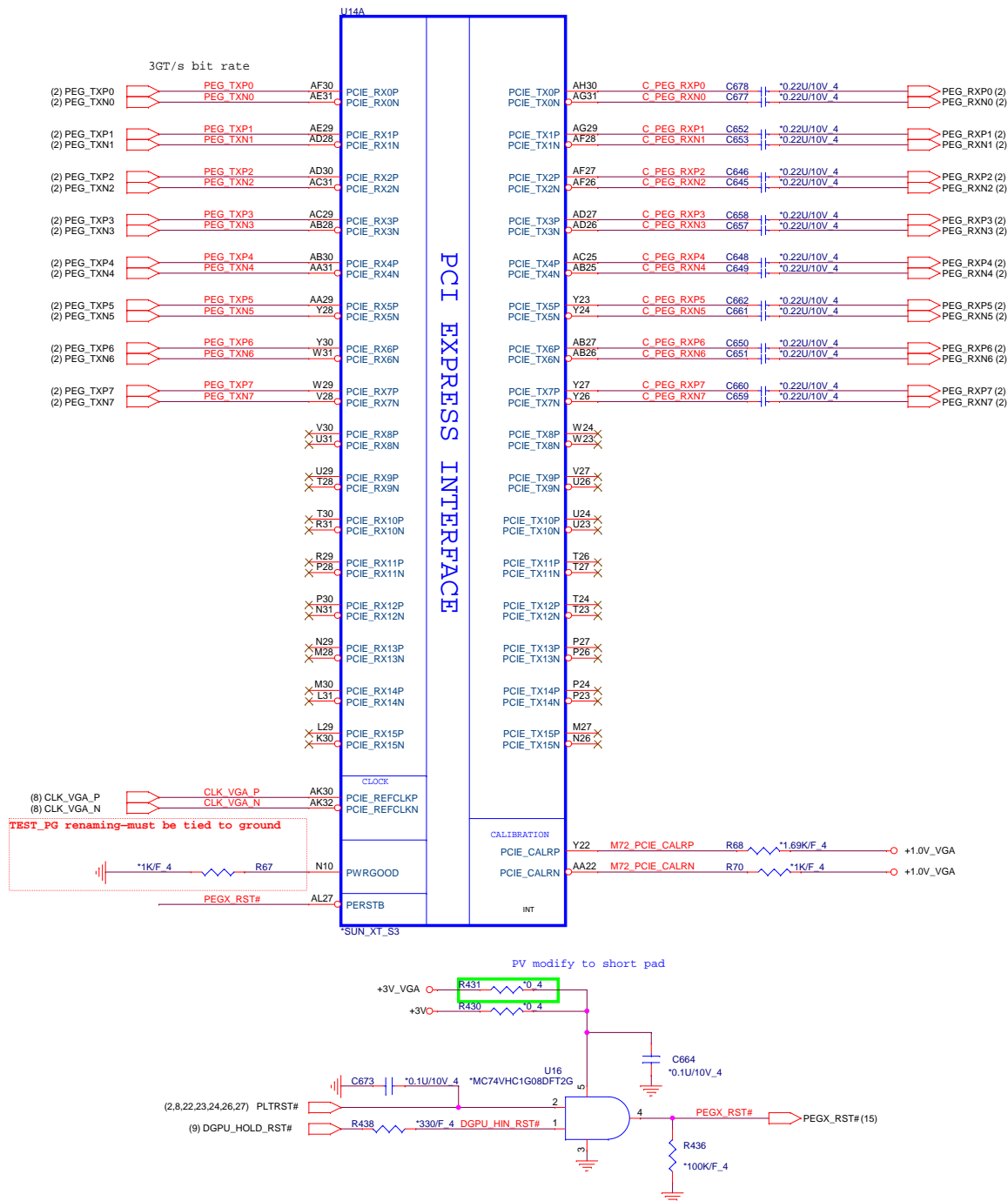


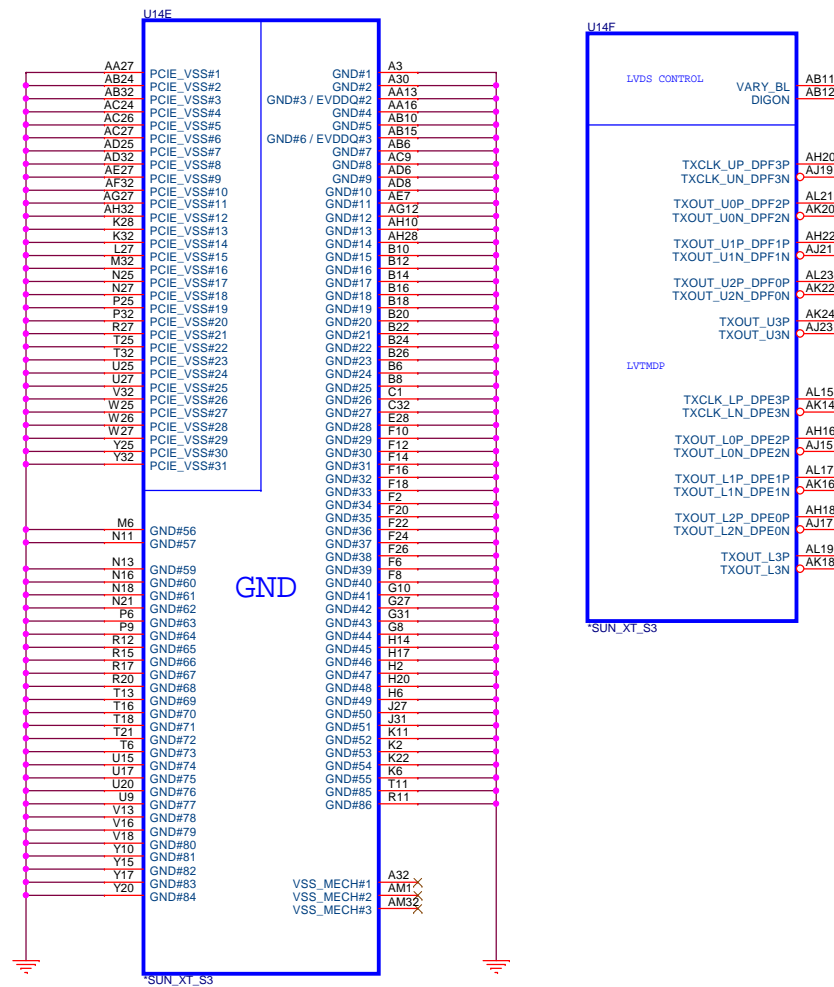
VREF DQ1 M1 Solution



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS(4.0H)	1A
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CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

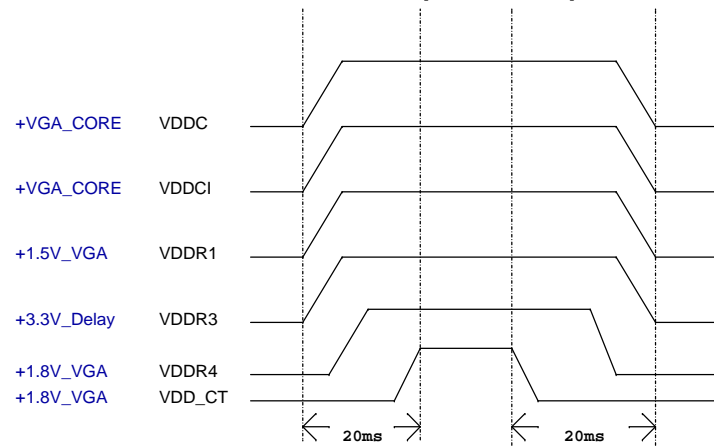
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIOQ[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

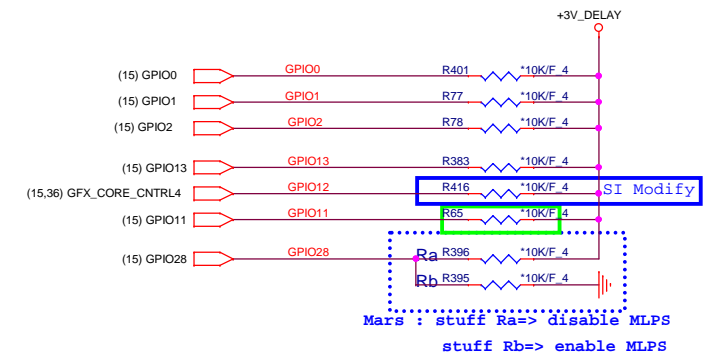
Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

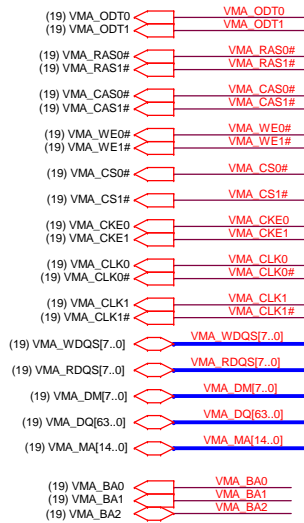
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



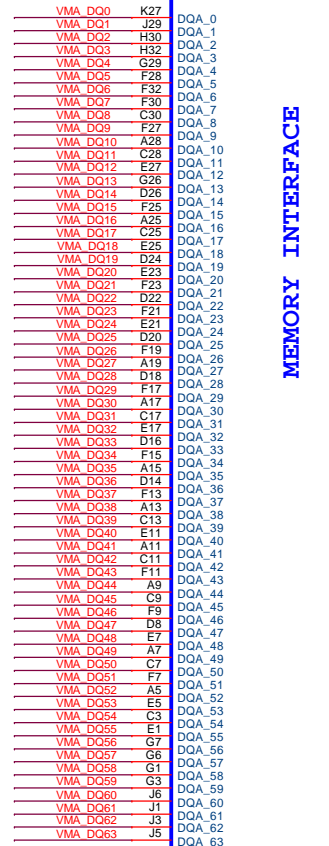
PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
Date: Friday, May 24, 2013	Sheet 16 of 37	

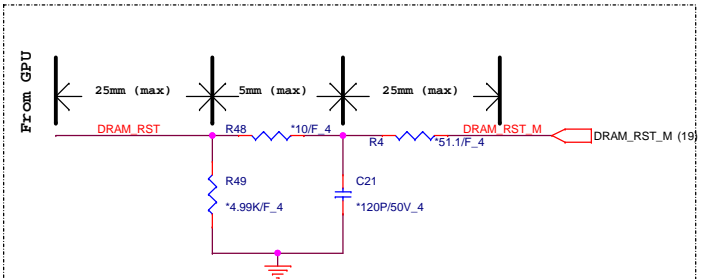
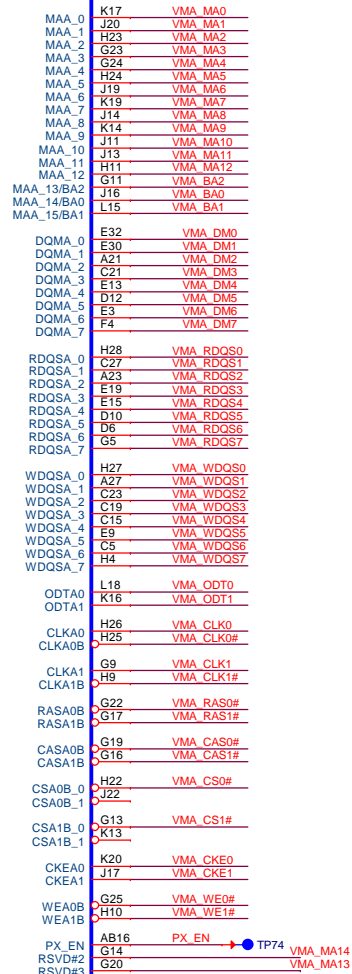




support 1gbt
VRAM (64M X 16)

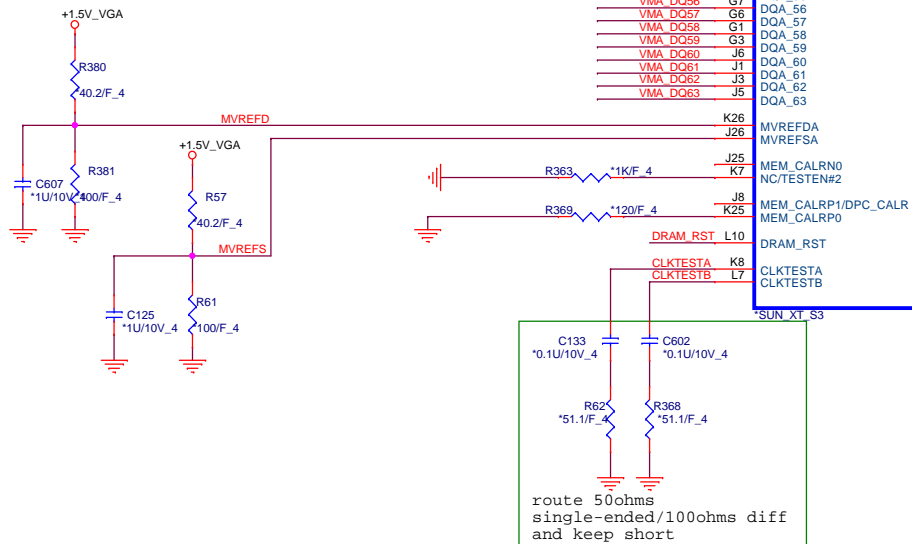


MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

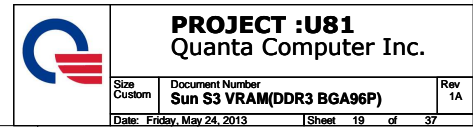


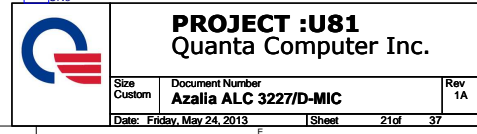
route 50ohms
single-ended/100ohms diff
and keep short

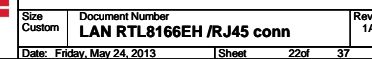


PROJECT :U81
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Size Custom	Document Number Sun S3 MEM_Interface	Rev 1A
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(8) PCIE_CLKREQ_CR# \Rightarrow PCIE_CLKREQ_CR# R331 0.4 PCIE_CLKREQ_CR#_R

(2,8,14,22,24,26,27) PLTRST# \Rightarrow PLTRST#

PCIE_CLKREQ_CR#_R

zdiff = 100 ohm

(8) CLK_PCIE_CRP
(8) CLK_PCIE_CRN
(8) PCIE_RXP3_CARD
(8) PCIE_RXN3_CARD

Please add 9 GND VIAS
connection with thermal PAD

Close to chip pin

12/13 CLK & D0-D3 Change to 33ohm for EMI

Close to chip pin

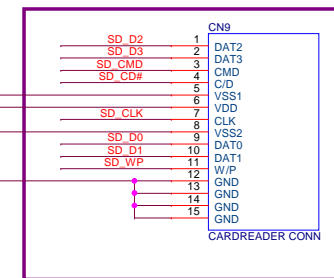
SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin

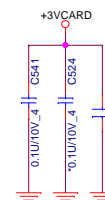
Reserve for EMI

SD_D0	EC21	5.6P/16V_4
SD_D1	EC20	5.6P/16V_4
SD_D2	EC30	5.6P/16V_4
SD_D3	EC29	5.6P/16V_4

SD / MMC
CARD READER



SI change PW to 11pin

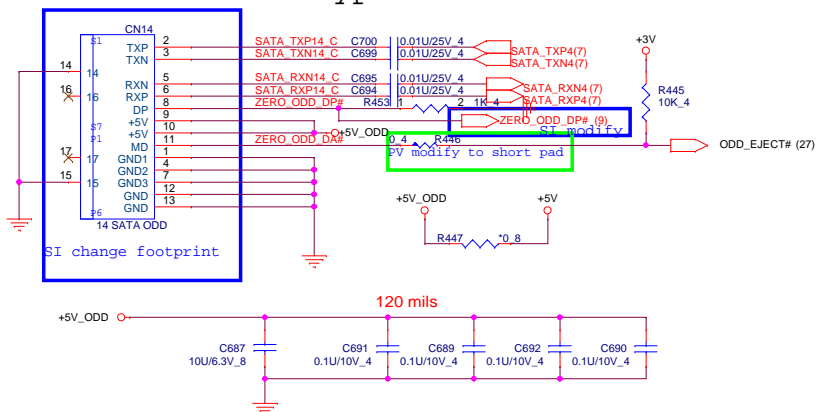


CLOSE CONN

SATA ODD
CONNECTOR

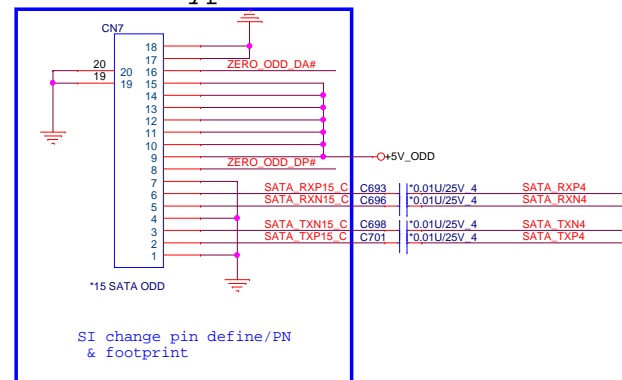
14" SATA ODD

Bypass CAP close conn



15" SATA ODD

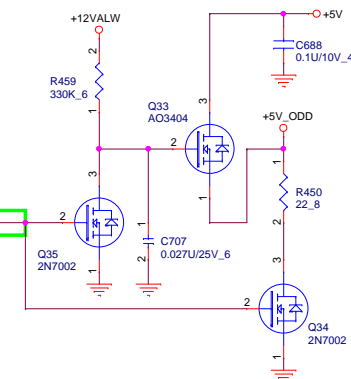
New Type



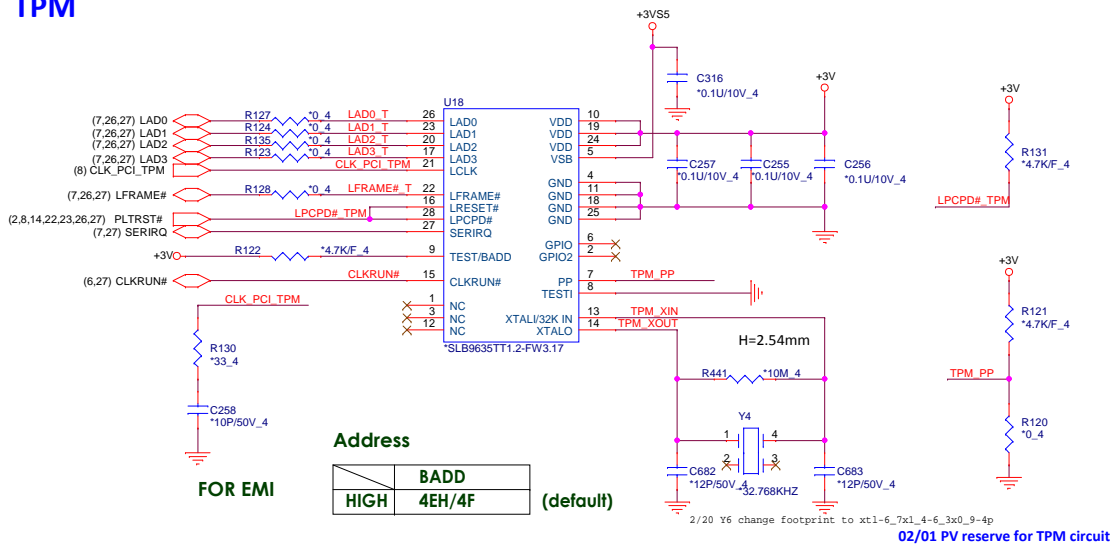
SI change pin define/PN
& footprint

PV modify to short pad
(27) ZERO_PWR_ODD \Rightarrow R458 0.4

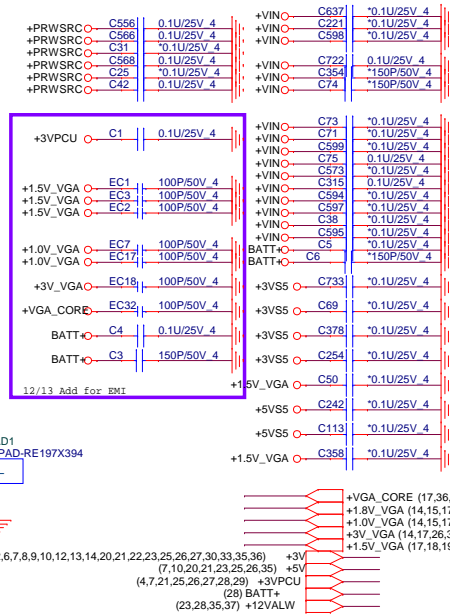
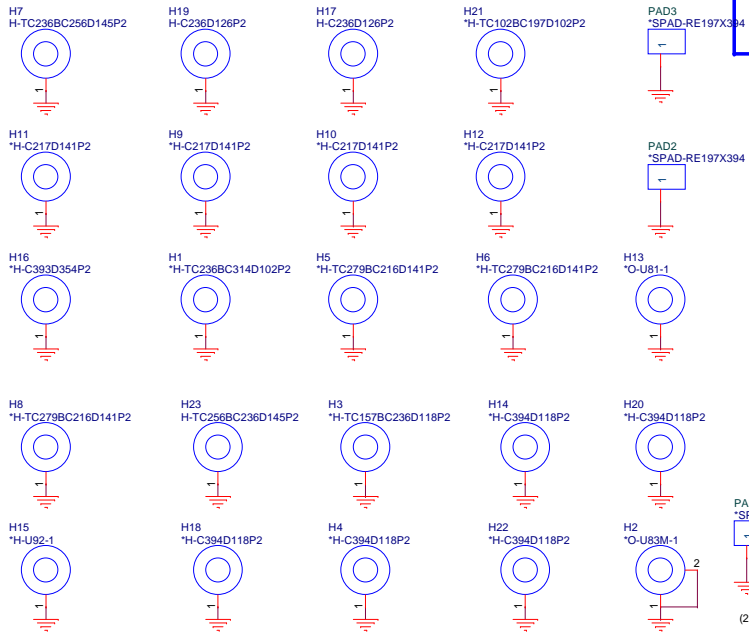
High : ODD power down
Low : ODD power on



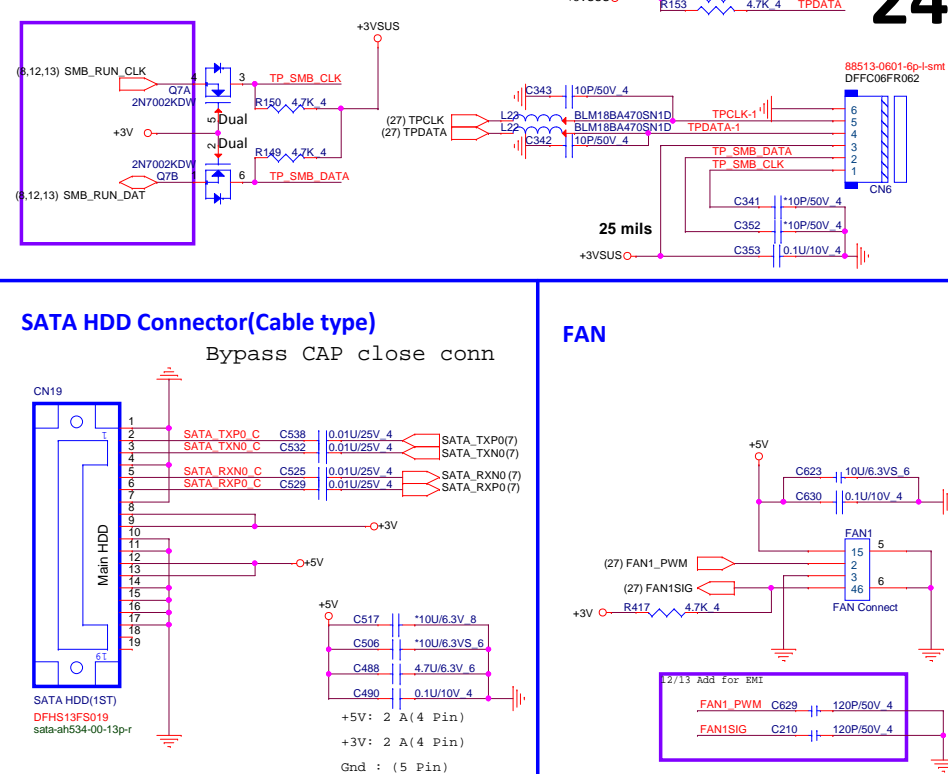
TPM



Hole



Touch Pad Connector



SATA HDD Connector(Cable type)

Bypass CAP close conn

FAN

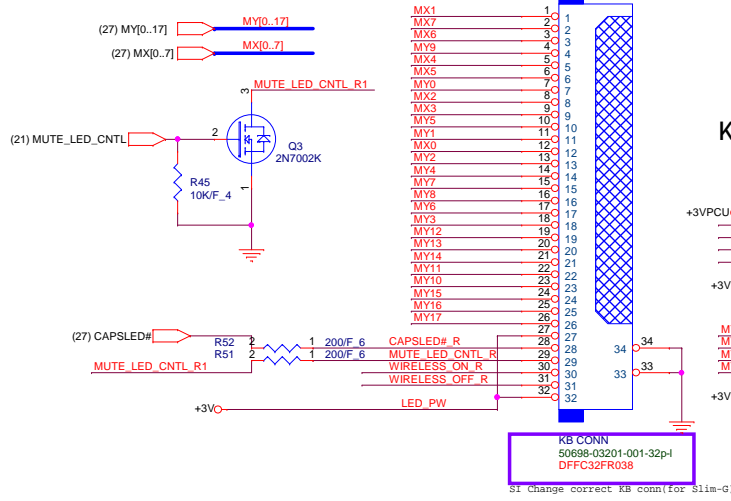
Mini PCI-E Card 2- Full size mSATA



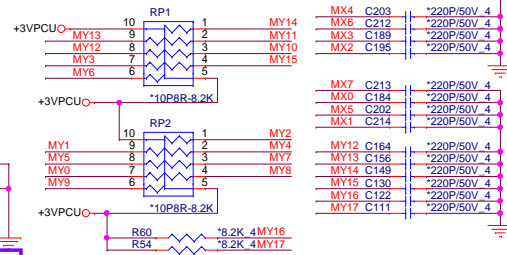
PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number HDD/mSATA/FAN/LED	Rev 1A
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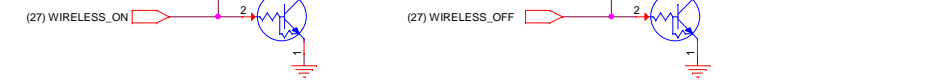
KEYBOARD Con.



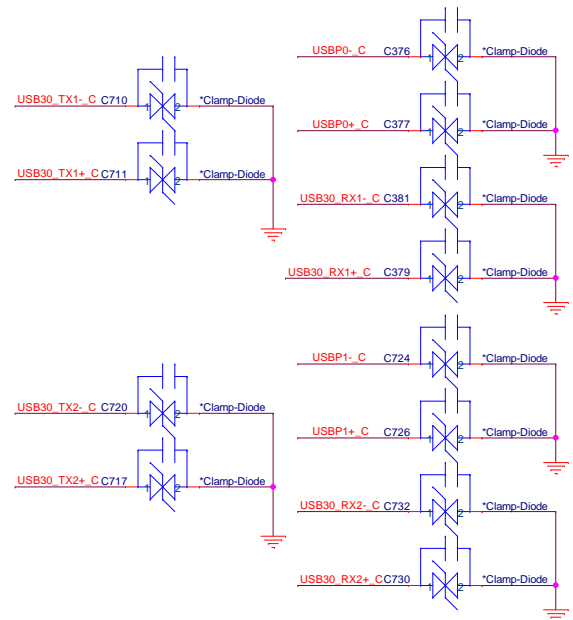
KEYBOARD PULL-UP



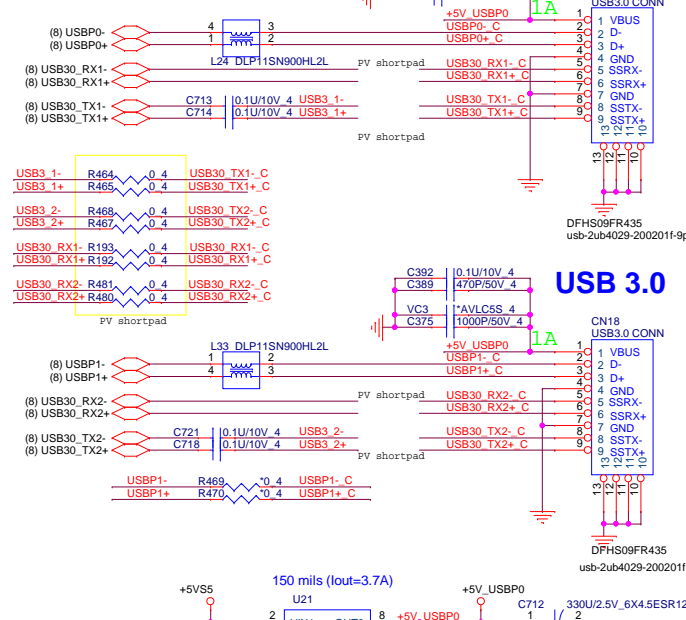
WIRELESS ON/OFF



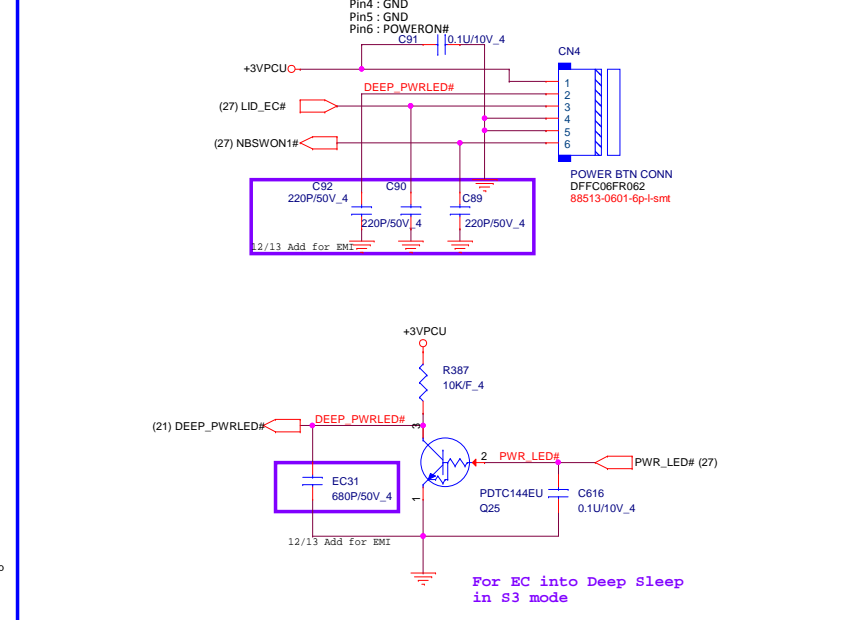
USB 2.0/3.0 Combo



USB 3.0



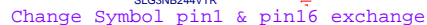
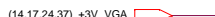
Power Button Connector



DEL TS 14" connector Circuit & Reserve +3V TS Power for AUO TS



(2,6,7,8,9,10,12,13,14,20,21,22,23,24,25,27,30,33,35,36)
(7,10,20,21,23,24,25,35)



Size Custom	Document Number WLAN/G-Sensor/G-CLK/TS	Rev 1A
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(6,22,27) PCIE_WAKE#

3 1 Q17 PDC144EU MINICAR_PME#

+3V_WLAN_P

10K R194 10K/F_4

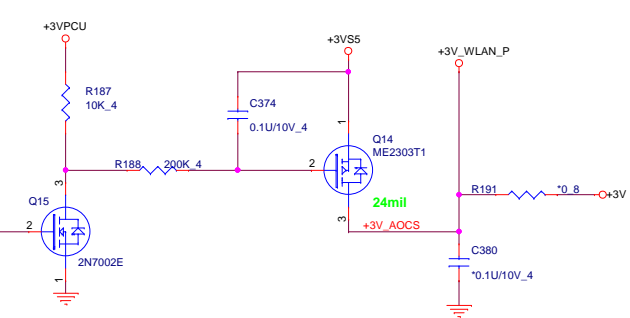
100nF C17

100nF C18

100nF C19

(27) EC_PCIE_WAKE#

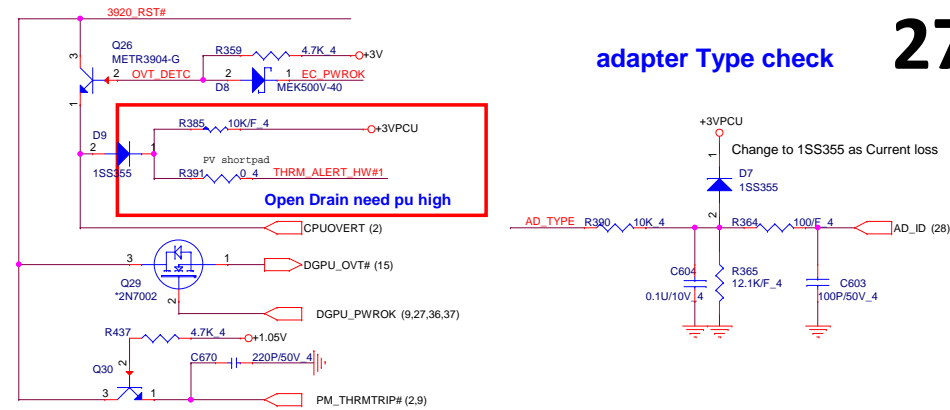
3 1 Q16 PDC144FI MINICAR_PME#



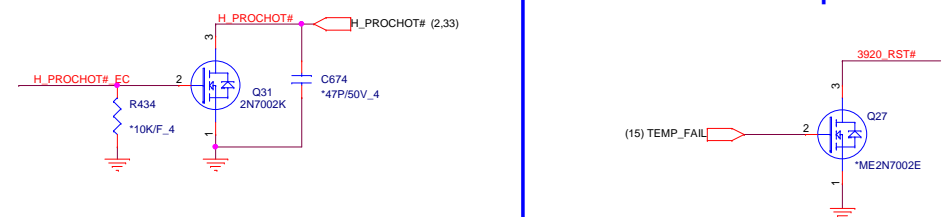
CLK 33M DEBUG EC19 *33P/50V 4

20mils width(min)

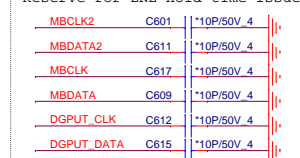
adapter Type check

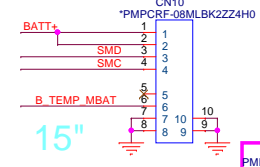


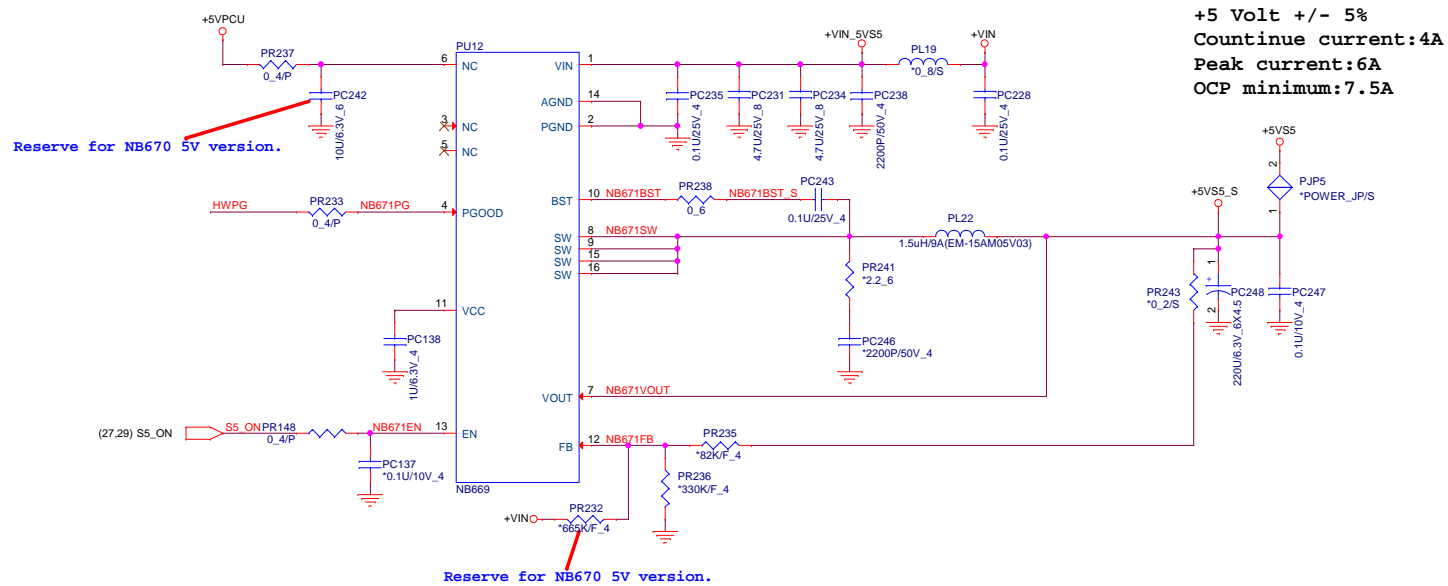
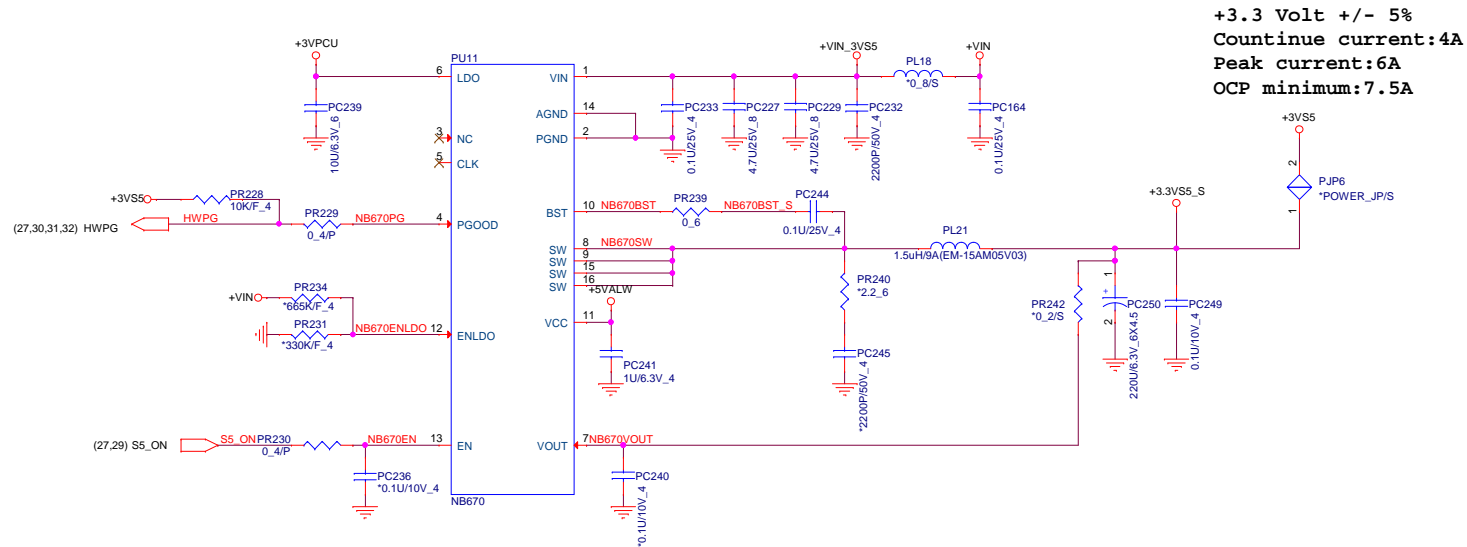
DGPU Thermal protect

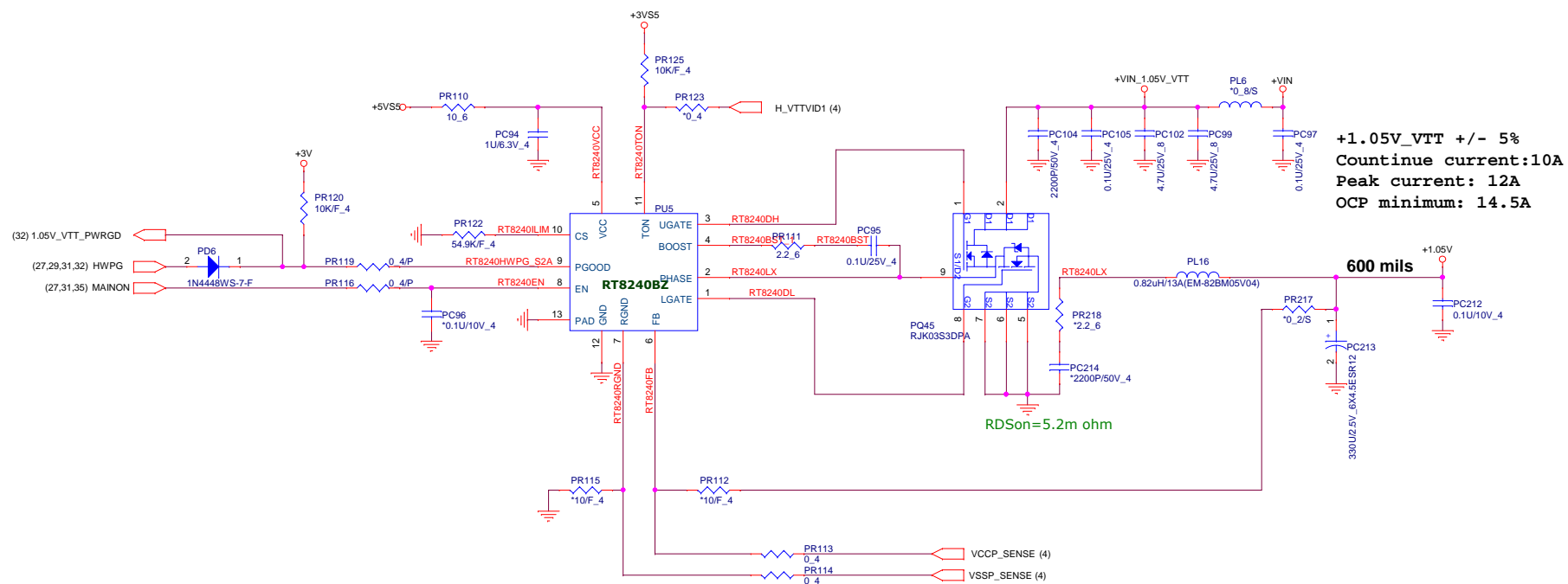


Reserve for ENE Hold time issue







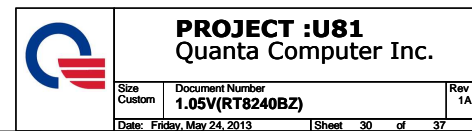


```
+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A
```

600 mils

$R_{DSon} = 5.2\text{m ohm}$

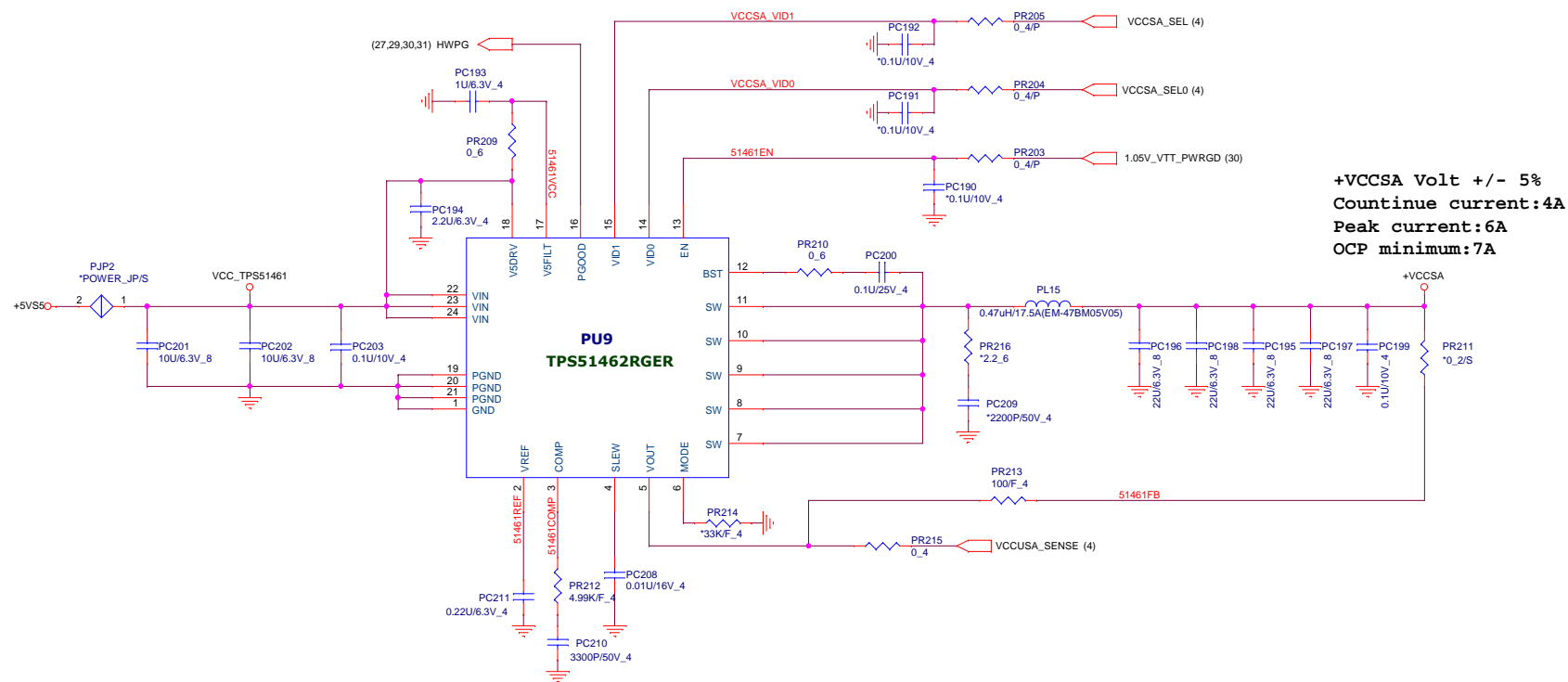
 +1.05V (2,4,6,7,8,10,26,27,33)

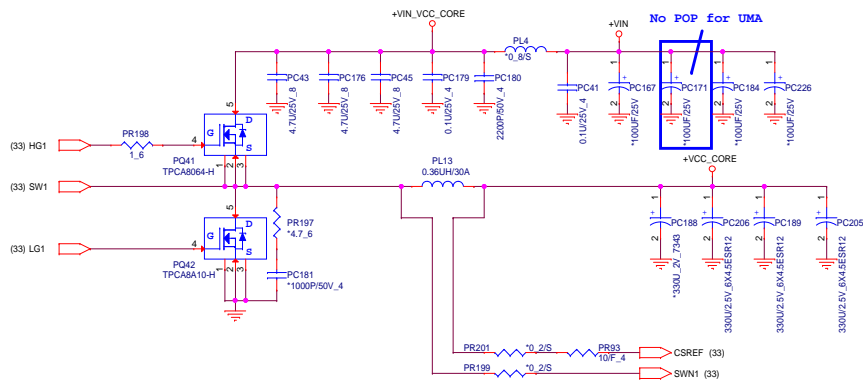


TPSS1462RGER/AL051462000

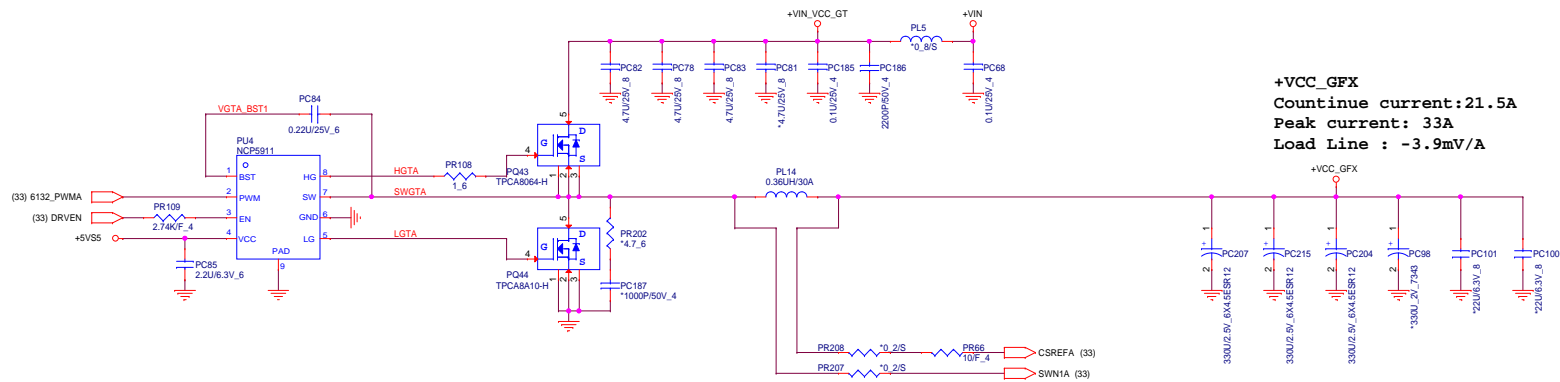
For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



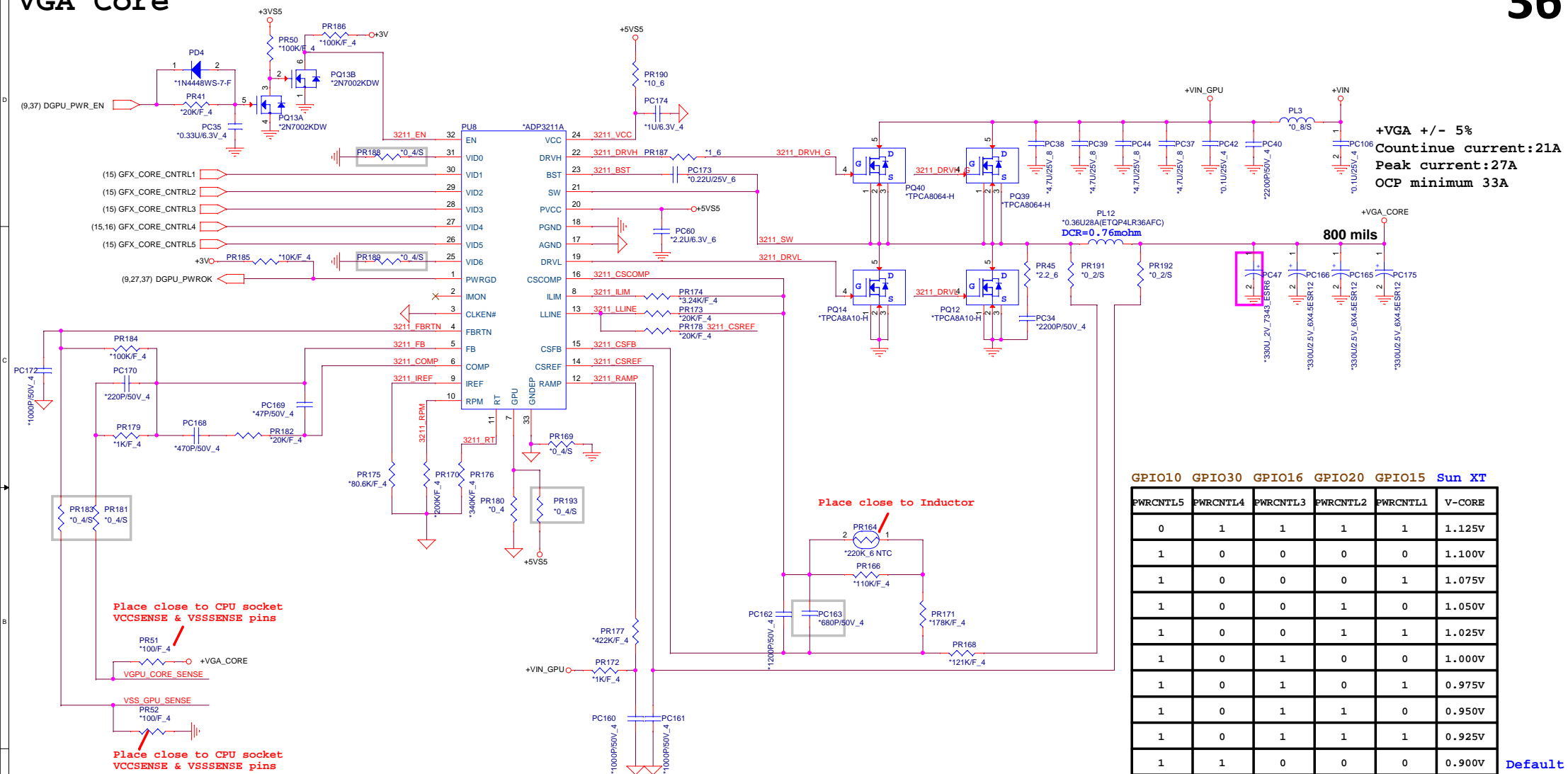


+VCC_CORE (ULV 17W)
 Countinue current:16A
 Peak current: 33A
 Load Line : -2.9mV/A



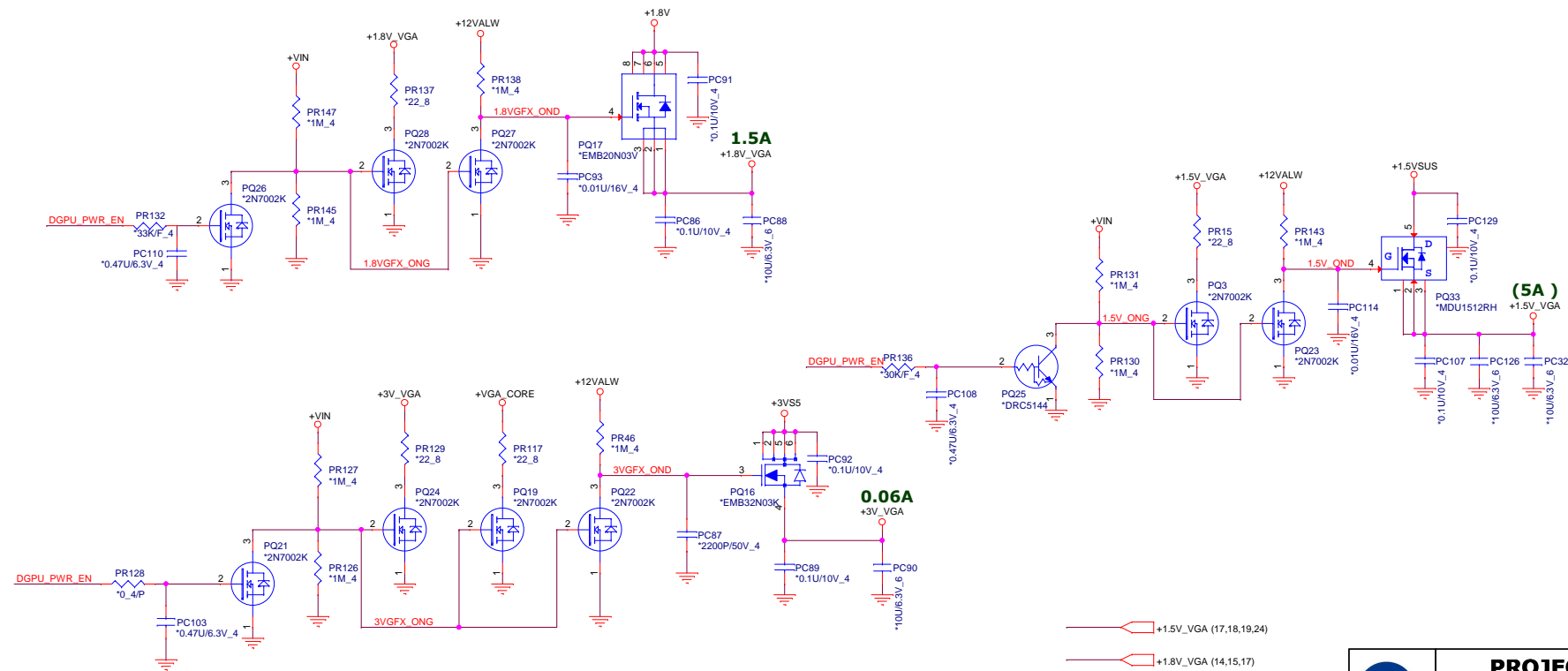
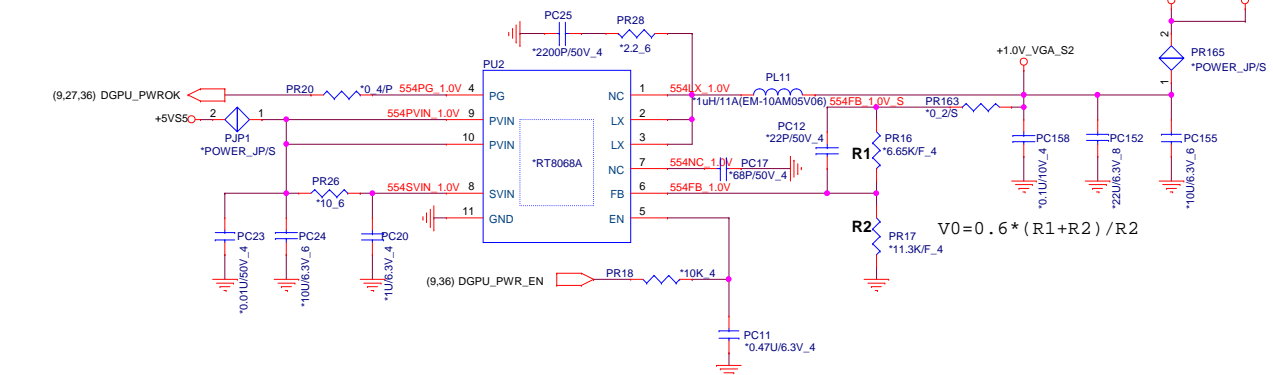
+VCC_GFX
 Countinue current:21.5A
 Peak current: 33A
 Load Line : -3.9mV/A





VGA Core



VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Continue current:2A
Peak current:3A
OCP minimum:4A



 +1.5V_VGA (17,18,19,24)
 +1.8V_VGA (14,15,17)
 +1.0V_VGA (14,15,17,24)
 +3V_VGA (14,17,24,26)



PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number +1.0V_VGA/1.8V_VGA/3V_VGA	Rev 1A
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